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CLAIMS 1-23. (CANCELLED)

24. A method of forming an integrated circuit device comprising:

providing a semiconductor substrate having a first portion and a second portion;

forming a gate stack comprising:

a gate dielectric formed over the first portion of the semiconductor substrate; and

a gate electrode formed over the gate dielectric;

forming a first patterned anti-reflective coating (ARC) over the gate stack;

forming a non-volatile memory stack comprising:

a charge storage layer formed over the second portion of the semiconductor substrate; and

a first dielectric layer formed over the charge storage layer;

forming a second patterned ARC over the non-volatile memory stack;

forming a second dielectric layer over the gate stack and the non-volatile memory stack;

removing portions of the second dielectric layer to form first spacers adjacent the gate stack and the non-volatile memory stack;

removing the first patterned ARC and the second patterned ARC after removing portions of the second dielectric layer;

forming a first channel under the gate stack; and

forming a second channel under the non-volatile memory stack.

25. The method of claim 24, further comprising:

forming a third dielectric layer over first spacers;

forming a fourth dielectric layer over the third dielectric layer;

removing portions of the third dielectric layer to form second spacers adjacent the first spacers; and

removing portions of the fourth dielectric layer to form third spacers adjacent the second spacers.

26. The method of claim 25, wherein removing the first patterned ARC and the second patterned ARC is before forming a third dielectric layer and forming a fourth dielectric layer.

27. The method of claim 26, wherein the second dielectric layer is densified prior to forming first spacers and removing the first patterned ARC and the second patterned ARC is a wet process.

28. The method of claim 27, wherein the second dielectric layer is an oxide, the third dielectric layer is an oxide, and the fourth dielectric layer is a nitride.

29. An integrated circuit device comprising:

a semiconductor substrate;

a stack comprising:

a patterned dielectric layer formed over the semiconductor substrate;

a patterned conductive layer formed over the patterned dielectric layer;

a first sidewall; and

a second sidewall, wherein the second sidewall is adjacent the first sidewall;

a first electrode region within the semiconductor substrate and adjacent the first sidewall;

a second electrode region within the semiconductor substrate and adjacent the second sidewall;

a channel region between the first electrode region and the second electrode region and under the stack;

oxide spacers adjacent the first sidewall and the second sidewall, wherein the oxide spacers have a first height; and

nitride spacers adjacent the first oxide spacers, wherein the nitride spacers have a second height which is less than the first height.

30. An integrated circuit device comprising:

a semiconductor substrate having a top surface;

a stack formed on the semiconductor substrate comprising:

a first layer;

a second layer formed over the first layer;

a first sidewall; and

a second sidewall opposite the first sidewall;

spacers adjacent the first sidewall and the second sidewall, wherein a first

portion of the top surface of the semiconductor substrate is under the spacers, a second portion is under the stack, and the first portion is substantially co-planar with the second portion;

a first doped region within the semiconductor substrate and adjacent the first sidewall;

a second doped region within the semiconductor substrate and adjacent the second sidewall; and

a channel region between the first doped region and the second doped region and within the semiconductor substrate.

31. The integrated circuit device of claim 30, wherein a first portion of the first and doped region and a second portion of the second doped region are under the gate dielectric.